A Translator Verification Technique for FPGA Software Development in Nuclear Power Plants

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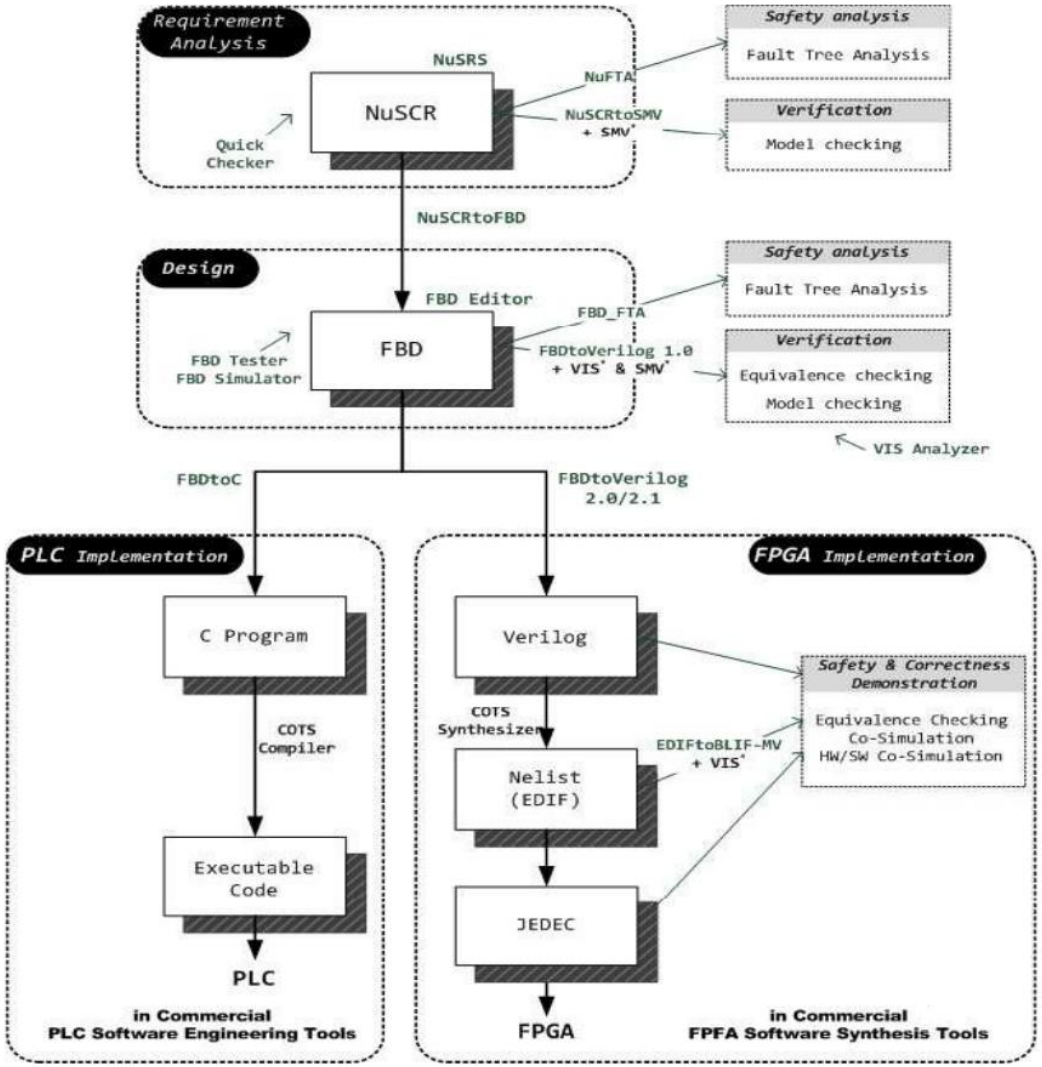
Introduction (1/2)

NuDE 2.0



Introduction (2/2)

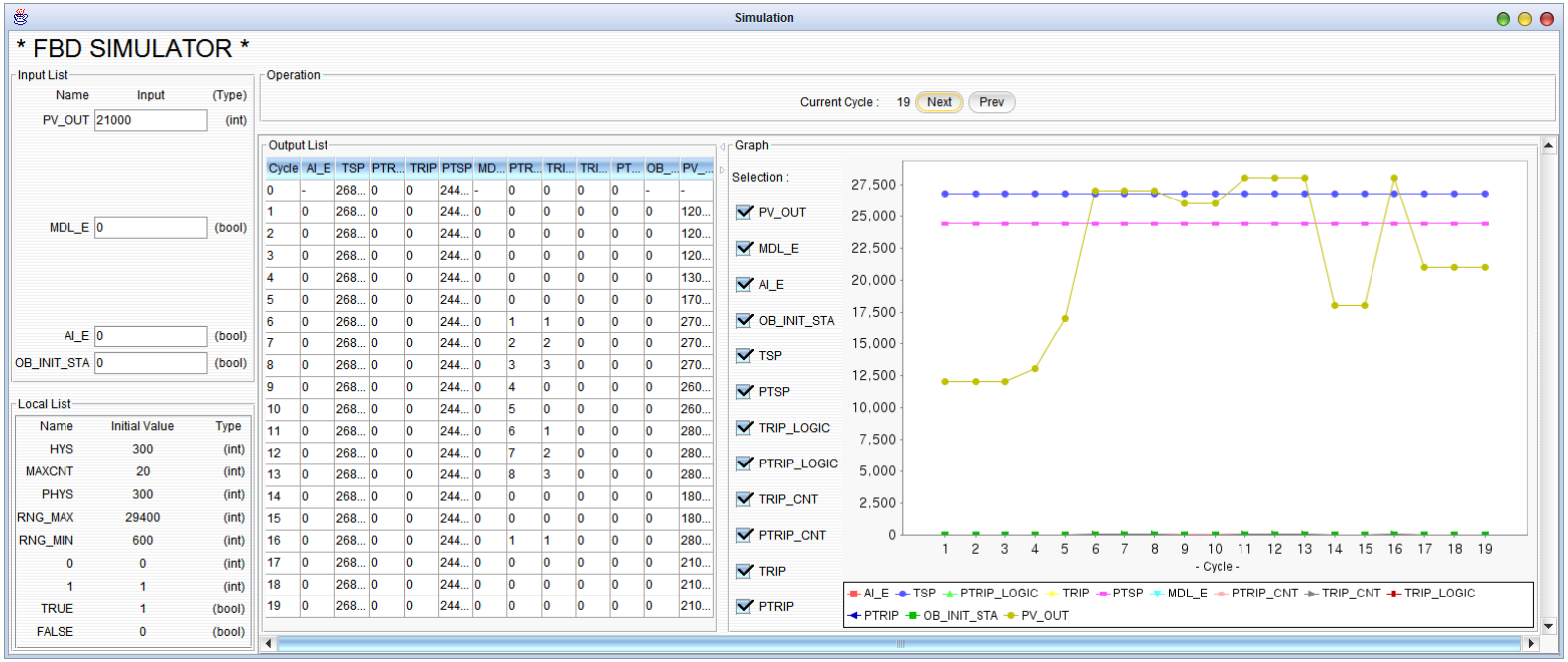
Verifying 'FBDtoVerilog'

- Co-Simulation technique can be used for demonstrating the correctness of translator such as 'FBDtoVerilog'
- For this co-simulation technique, many tools run separately such as 'Scenario Generator', 'FBD Simulator'
- We had develop integrated tool to support the co-simulation

Background(1/3)

FBD Simulator

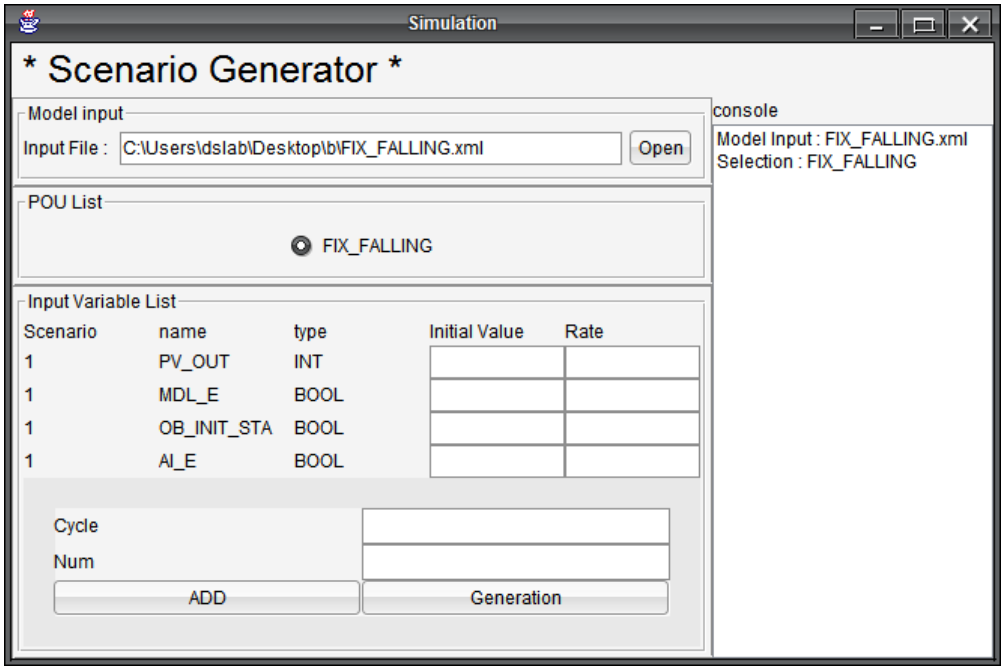
- Simulator for FBD
- Automatically classifies the POU (Program of Unit) in the FBD
- It presents input, output and local variable lists



Background(2/3)

Scenario Generator

- A tool that automatically generate an infinite number of scenarios
- Input is FBD
- It reflects the features of the domain such as range of value



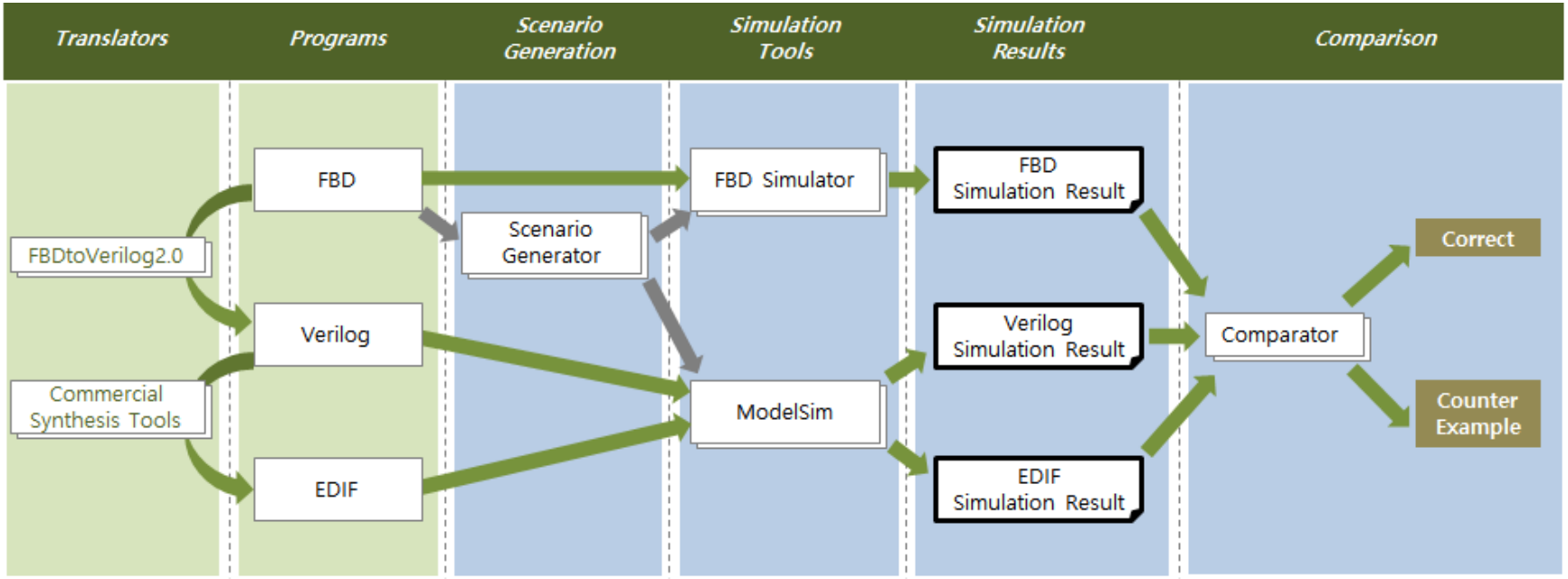
Background(3/3)

Co-Simulation

- Indirect verification technique
- It simulates programs with same scenario and compares results of simulation for confirming correctness
- Confirmation of correctness with co-simulation can make to enhance the reliability of the program

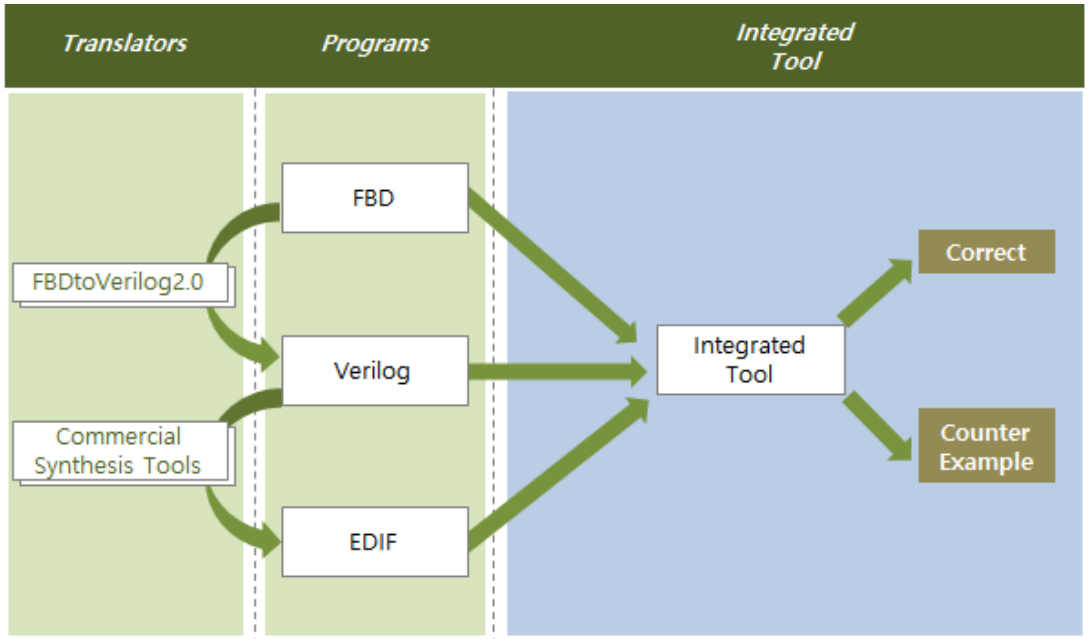
The Integrated Tool for Demonstrating the Correctness of Translator

Overall Process – Before Using Integrated Tool



The Integrated Tool for Demonstrating the Correctness of Translator

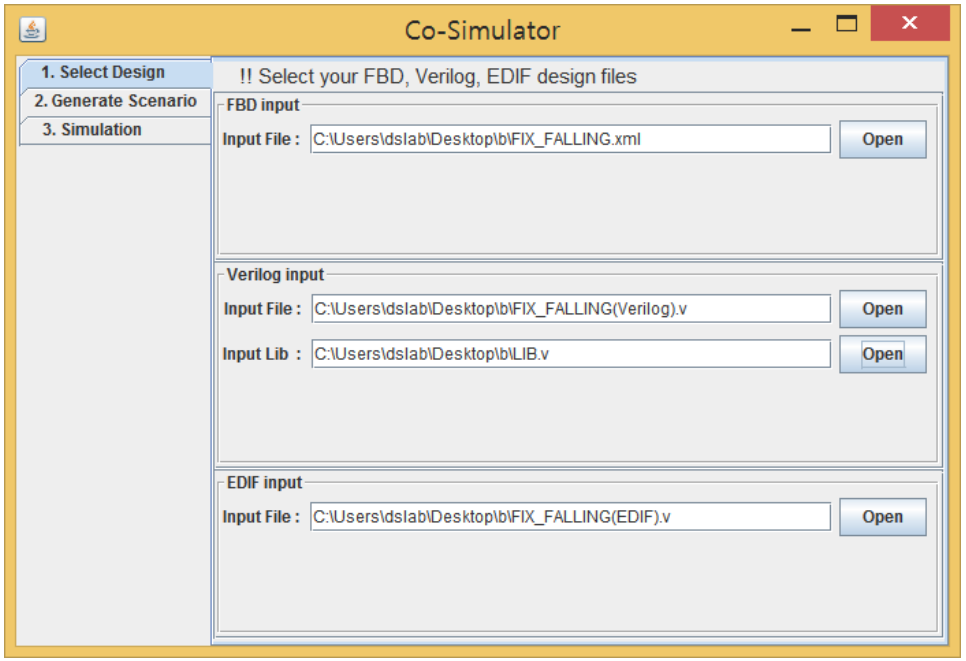
Overall Process – Using Integrated Tool



The Integrated Tool for Demonstrating the Correctness of Translator

Input programs

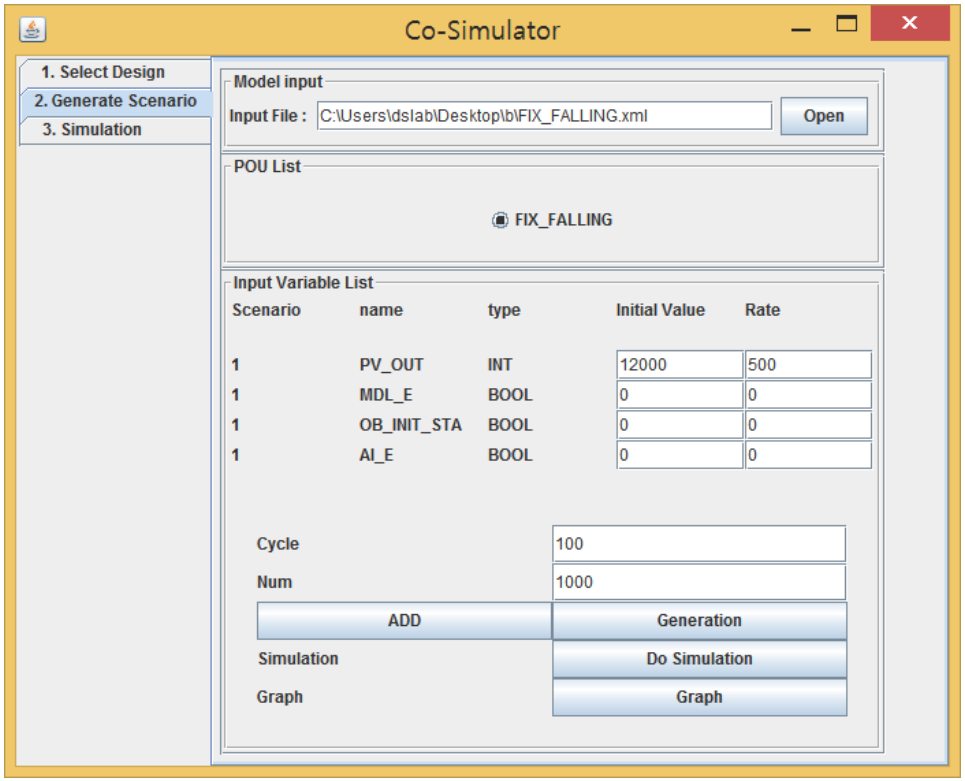
- FBD
- Verilog
- EDIF



The Integrated Tool for Demonstrating the Correctness of Translator

Scenario Generation

- Use 'Scenario Generator'
- Create script (.do file) for automatically use of ModelSim



The Integrated Tool for Demonstrating the Correctness of Translator

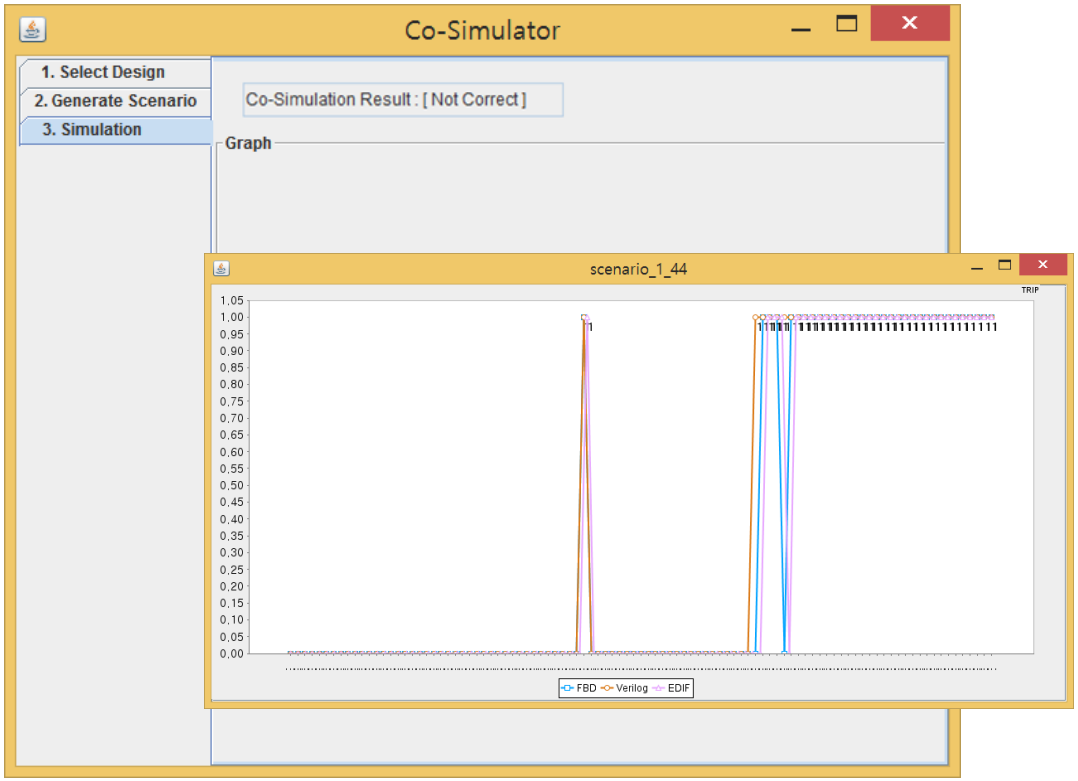
- ModelSim Script (.do file)

```
quietly set ACTELLIBNAME proasic3e

if {[file exists presynth/_info]} {
 echo "INFO: Simulation library presynth already exists"
    } else {
    file delete -force presynth
    vlib presynth
 }
vmap presynth presynth
vmap proasic3e "C:/Microsemi/Libero_v11.4/Designer/lib/modelsim/precompiled/vlog/proasic3e"

vlog -work presynth "C:/Users/dslab/Desktop/myfile.v"
vlog -work presynth "C:/Users/dslab/Desktop/test 1001/hdl/LIB.v"

vlog "+incdir+C:/Users/dslab/Desktop/result" -work presynth "C:/Users/dslab/Desktop/result/verilog_Test_Benchs_for_scenario/scenario_1/scenario_1_0.v"
vsim -L proasic3e -L presynth -t 1ps presynth.scenario_1_0
add wave /scenario_1_0/*
run 1000us
add list -decimal *
write list C:/Users/dslab/Desktop/result/scenario_1_0_verilog.lst
vlog "+incdir+C:/Users/dslab/Desktop/result" -work presynth "C:/Users/dslab/Desktop/result/verilog_Test_Benchs_for_scenario/scenario_1/scenario_1_1.v"
vsim -L proasic3e -L presynth -t 1ps presynth.scenario_1_1
add wave /scenario_1_1/*
run 1000us
add list -decimal *
write list C:/Users/dslab/Desktop/result/scenario_1_1_verilog.lst
```

The Integrated Tool for Demonstrating the Correctness of Translator

Simulation & Comparison

- Simulation
- Comparison
- Result
  - Correct
  - Not Correct
    - → Counter example



The Integrated Tool for Demonstrating the Correctness of Translator

- Simulation result file

```
Name begin
scenario_1_1
end

Outputs begin
TSP PTRIP_LOGIC TRIP    PTSP    PTRIP_CNT   TRIP_CNT    TRIP_LOGIC  PTRIP
end

Feedback begin
TSP PTRIP_LOGIC PTSP    PTRIP_CNT   TRIP_CNT    TRIP_LOGIC
end

Result begin
26805   0   0   24429   1   0   0   0
26805   0   0   24429   2   0   0   0
26805   0   0   24429   3   0   0   0
26805   0   0   24429   4   0   0   0
26805   0   0   24429   5   0   0   0
26805   0   0   24429   6   0   0   0
26805   0   0   24429   7   0   0   0
26805   0   0   24429   8   0   0   0
26805   0   0   24429   0   0   0   0
26805   0   0   24429   0   0   0   0
26805   0   0   24429   0   0   0   0
26805   0   0   24429   0   0   0   0
26805   0   0   24429   1   0   0   0
26805   0   0   24429   2   0   0   0
26805   0   0   24429   3   0   0   0
26805   0   0   24429   4   0   0   0
26805   0   0   24429   5   0   0   0
26805   0   0   24429   6   0   0   0
26805   0   0   24429   7   0   0   0
```

<FBD Simulation result>

ps	delta	/scenario_1_0/SYSCLK	/scenario_1_0/NSYSRESET	/scenario_1_0/pulse	/scenario_1_0/PV_OUT	/scenario_1_0/MDL_E	/scenario_1_0/AI_E	/scenario_1_0/OB_INIT_STA	/scenario_1_0/TSP	/scenario_1_0/PTSP	/scenario_1_0/TRIP_CNT	/scenario_1_0/PTRIP_CNT	/scenario_1_0/TRIP_LOGIC	/scenario_1_0/PTRIP_LOGIC	/scenario_1_0/TRIP	/scenario_1_0/PTRIP
0	+0	0	0	0	0	26000	0	0	0	0	x	x	x	x	x	x
50000	+0	-1	0	0	0	26000	0	0	0	0	x	x	x	x	x	x
100000	+0	0	0	0	0	26000	0	0	0	0	x	x	x	x	x	x
150000	+0	-1	0	0	0	26000	0	0	0	0	x	x	x	x	x	x
200000	+0	0	0	0	0	26000	0	0	0	0	x	x	x	x	x	x
250000	+0	-1	0	0	0	26000	0	0	0	0	x	x	x	x	x	x
300000	+0	0	0	0	0	26000	0	0	0	0	x	x	x	x	x	x
350000	+0	-1	0	0	0	26000	0	0	0	0	x	x	x	x	x	x
400000	+0	0	0	0	0	26000	0	0	0	0	x	x	x	x	x	x
450000	+0	-1	0	0	0	26000	0	0	0	0	x	x	x	x	x	x
500000	+0	0	0	0	0	26000	0	0	0	0	x	x	x	x	x	x
550000	+0	-1	0	0	0	26000	0	0	0	0	x	x	x	x	x	x
600000	+0	0	0	0	0	26000	0	0	0	0	x	x	x	x	x	x
650000	+0	-1	0	0	0	26000	0	0	0	0	x	x	x	x	x	x
700000	+0	0	0	0	0	26000	0	0	0	0	x	x	x	x	x	x
750000	+0	-1	0	0	0	26000	0	0	0	0	x	x	x	x	x	x
800000	+0	0	0	0	0	26000	0	0	0	0	x	x	x	x	x	x
850000	+0	-1	0	0	0	26000	0	0	0	0	x	x	x	x	x	x
900000	+0	0	0	0	0	26000	0	0	0	0	x	x	x	x	x	x
950000	+0	-1	0	0	0	26000	0	0	0	0	x	x	x	x	x	x
1000000	+0	-1	*	0	0	26000	0	0	0	0	x	x	x	x	x	x
1000000	+1	0	*	0	0	26000	0	0	0	0	x	x	x	x	x	x
1000300	+0	0	*	0	0	26000	0	0	0	26805	24429	0	0	0	0	0
1050000	+0	-1	*	0	0	26000	0	0	0	26805	24429	0	0	0	0	0
1100000	+0	0	*	0	0	26000	0	0	0	26805	24429	0	0	0	0	0

<ModelSim Simulation result>

Case Study

- KNICS RPS BP

	FIX_FALLING	FIX_RISING	MANUAL_RATE_FALLING	VARIABLE_FALLING	VARIABLE_RISING
Scenario	1000	1000	1000	1000	1000
Initial Values	12000	26000	15000	15000	15000
Rate of Change	500	500	500	100	100
Cycles	100	100	100	100	100
Time	57:07	56:50	1:08:13	59:03	58:56

Total 5000 scenario / All Correct

Conclusion and future work

- We developed the integrated tool in order to automatically perform the co-simulation
- We demonstrated the correctness of translator
  - 'FBDtoVerilog2.0'
  - 'Synplify Pro'

- We plan to extend the integrated tool to verify VHDL
- And plan to elaborate the scenarios on the basis of adequate coverage criteria in order to increase the confidence of verification

THANK YOU